Critique for "Power Savings in Embedded Processors through Decode Filter Cache"

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This paper proposes a mechanism to reduce the instruction fetch and decode power in the pipeline. The new cache, DFC (Decode Filter Cache), stores the already decoded instructions and prevents decoding and fetching the same instructions repeatedly. This gives an overall reduction in decode and fetch power.

Strengths:

1> The DFC and the Line buffer run in parallel with the I-cache. Thus, the performance overhead of the implementation is less. The authors claim the performance overhead of around 1%.

2> The simulation results show a 34% reduction in power. This reduction is substantial compared to the performance overhead.

Weaknesses:

1> The predictor does not run in parallel with the pipeline. The performance overhead on cycle times for instructions due to the predictor is neither presented nor quantified.

2> The authors do not clearly explain how they classify instructions on the basis of profiling. No information is given about which benchmarks are used for calculating frequency and why the particular benchmarks are used.

3> They do not provide any values of width and frequency for optimal cacheable/non-cacheable classification.

4> The DFC, predictor, Line buffer will lead to significant hardware overhead in the pipeline.

5> The authors give the scenarios in which mis-predictions can occur. But no information is provided about handling mis-predictions and overhead of mis-predictions.

6> The DFC does not have inherent spatial locality. To incorporate spatial locality Line buffer is used. This results in greater hardware overhead.