Introduction

In order to save energy when the CPU is idle, the CPU can be commanded to enter a low-power mode. Each CPU has several power modes and they are collectively called “C-states” or “C-modes”. In this tutorial we will explain what these modes are, what they do and the modes supported by each processor.

The lower-power mode was first introduced with the 486DX4 processor, so this concept is far from being new. With time, however, more power modes were introduced and enhancements were made to each mode so the CPU could consume less power when it is one of these low-power modes.

The basic idea of these modes is to cut the clock signal and power from idle units inside the CPU. The more units you stop (by cutting the clock), reduce the voltage or even completely shut down, more energy you save, but more time is required for the CPU to “wake up” and be again 100% operational.

These modes are known as “C-states”. They are numbered starting at C0, which is the normal CPU operating mode, i.e., the CPU is 100% turned on. The higher the C number is, deeper is the CPU sleep mode, i.e., more circuits and signals are turned off and more time the CPU will take to go back to C0 mode, i.e., to wake-up.

Each mode is also known by a name and several of them have sub-modes with different power saving – and thus wake-up time – levels.

In the table below we summarize all C-state modes currently available. Modes C1 to C3 work by basically cutting clock signals used inside the CPU, while modes C4 to C6 work by reducing the CPU voltage. “Enhanced” modes can do both at the same time.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Name</th>
<th>What it does</th>
<th>CPUs</th>
</tr>
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<tbody>
<tr>
<td>C0</td>
<td>Operating State</td>
<td>CPU fully turned on</td>
<td>All CPUs</td>
</tr>
<tr>
<td>C1</td>
<td>Halt</td>
<td>Stops CPU main internal clocks via software; bus interface unit and APIC are kept running at full speed.</td>
<td>486DX4 and above</td>
</tr>
<tr>
<td>C1E</td>
<td>Enhanced Halt</td>
<td>Stops CPU main internal clocks via software and reduces CPU voltage; bus interface unit and APIC are kept running at full speed.</td>
<td>All socket 775 CPUs</td>
</tr>
<tr>
<td>C1E</td>
<td>—</td>
<td>Stops all CPU internal clocks.</td>
<td>Turion 64, 65-nm Athlon X2 and Phenom CPUs</td>
</tr>
<tr>
<td>C2</td>
<td>Stop Grant</td>
<td>Stops CPU main internal clocks via hardware; bus interface unit and APIC are kept running at full speed.</td>
<td>486DX4 and above</td>
</tr>
<tr>
<td>C2</td>
<td>Stop Clock</td>
<td>Stops CPU internal and external clocks via hardware</td>
<td>Only 486DX4, Pentium, Pentium MMX, K5, K6, K6-2, K6-III</td>
</tr>
</tbody>
</table>
Now we are going to explain each C-state in details.

### C1 State

All x86 CPUs have an instruction called “HLT” (“Halt”), where the CPU remains “stopped”, idle, doing nothing when it is ran. The CPU is put back to life after it receives an interruption, which is a hardware signal that tells the CPU to stop what it is doing at the moment and take care of the hardware device that sent that signal.

Since in halt mode the CPU is completely idle, Intel decided that this would be the perfect place to reduce the CPU power consumption, so they added the “Halt” or “Auto Halt” mode – now known as the C1 state – starting on the 486DX4 processor. All CPUs after 486DX4 from both Intel and AMD implement this mode, and also the “SL Enhanced” version of 486DX2.

So after the program runs an HLT instruction, the CPU enters its traditional halt mode but now the internal CPU clock signal is stopped (only two units inside the CPU continue to be fed with the CPU internal clock, the bus interface unit and the Advanced Programmable Interrupt Controller, APIC; this is done to allow the CPU to temporarily exit the Halt state if an important request comes through the CPU external bus). As soon as the CPU receives an interruption signal it goes back to its normal operating state, with the clock signal being restored.

Since the clock signal is stopped for almost all CPU internal units, they stop running, making them to consume less power.

Interesting enough no special programming is required for the CPU to enter the C1 state, as HLT instruction is present since the first 8086 CPU. Before the 486DX4 the HLT instruction was used basically to stop the CPU and make it wait for an interruption. After this CPU, programmers could use this mode to put the CPU into a lower power consumption state.

As mentioned, the CPU can temporarily leave the Halt (C1) state to deal with an important request coming from through the CPU external bus. This temporary leave is called Stop Clock Snoop State, HALT/Grant Snoop State or simply Snoop State and during its duration the CPU clock is restored. After this CPU has handled the request, it goes automatically back to the Halt (C1) state.

All Intel CPUs based on socket 775 (e.g., Pentium 4, Core 2 Duo) have an advanced Halt state called...
Enhanced Halt (naming used with Pentium 4 CPUs), Extended Halt (naming used with Core 2 Duo CPUs) or simply C1E, which also reduces the CPU voltage besides stopping the CPU internal clock. If this mode is enabled on the motherboard BIOS, the CPU will enter this mode instead of the traditional Halt (C1) mode when a HLT instruction is issue. Otherwise the CPU will continue to use the standard Halt mode.

Core 2 Duo also introduced the Extended Halt/Stop Grant Snoop state, which allows the CPU to temporarily exit C1E or C2E modes to respond to an important request coming from the CPU external bus, but keeping the CPU lower voltage instead of restoring the CPU full voltage.

Pay attention because AMD also uses the name C1E for a completely different thing. On their 65-nm Athlon X2 and Phenom CPUs C1E state works just like the C3 state, shutting down all CPU clocks. The CPU enters C1E state when this option is enabled on BIOS and all CPU cores enter the regular C1 (Halt) state. When this happens, the automatically CPU switches to this C1E state in order to save energy. The difference between AMD's C1E and C3 states is basically how the CPU enters the Sleep state: while on the traditional C3 state the CPU must be put in that state usually by a command from the operating system, on C1E the CPU enters the Sleep state automatically when all cores are at Halt (C1) state.

C2 State

The C2 state was also introduced with 486DX4, by adding one extra pin to the CPU, called “STPCLK” (“Stop Clock”). When this pin is activated, the CPU core clock is cut.

As you can see, C2 state is somewhat similar to C1 state: both cut the CPU core clock. The difference between them is how the CPU achieves this: C1 state is activated by software (through an “HLT” instruction) while C2 state is activated by hardware (by sending a signal to a CPU pin called “STPCLK”).

Like it happens when the CPU is in the C1 state, the CPU internal clock isn't completely stopped when the CPU enters C2 state: the bus interface and APIC units are still being fed with the CPU internal clock rate. This is done to allow the CPU to temporarily exit the C2 state to take care of an important request coming from the CPU external bus.

Since the clock signal is stopped for almost all CPU internal units, they stop running, making them to consume less power.

There are two sub-modes for the C2 state: Stop Grant and Stop Clock. Stop Grant is achieved after the “STPCLK” pin is activated. As explained, in this mode the CPU core clock is stopped but the clock generator chip (also known as PLL, Phase-Locked Loop) is still active and generating the external bus reference clock, i.e., the CPU external clock.

486DX4, Pentium, Pentium MMX, K5, K6, K6-2 and K6-III could go one step further and enter a deeper sub-state called Stop Clock where the clock generator chip would be turned off and thus the external clock signal would also be turned off, thus saving more energy. Current CPUs don't have the Stop Clock mode inside the C2 State but on the C3 Deep Sleep state.

Like the Halt (C1) state, the CPU can temporarily leave the Stop Grant (C2) state to deal with an important request coming from through the CPU external bus. This temporary leave is called Stop Clock Snoop State, HALT/Grant Snoop State or simply Snoop State and during its duration the CPU clock is restored. After the CPU has handled the request, it goes automatically back to the Stop Grant (C2) state.

Core 2 Duo CPUs brought an advanced Stop Grant state called Extended Stop Grant or C2E, which also reduces the CPU voltage besides stopping the CPU internal clock. If this mode is enabled on the motherboard BIOS, the CPU will enter this mode instead of the traditional Stop Grant (C2) mode when STPCLK pin is activated. Otherwise the CPU will continue to use the standard Stop Grant mode.

This CPU also introduced the Extended Halt/Stop Grant Snoop state, which allows the CPU to temporarily exit C1E or C2E modes to respond to an important request coming from the CPU external bus, but keeping the CPU lower voltage instead of restoring the CPU full voltage.

C3 State

C3, also known as Sleep state, was first used on Pentium II from Intel and the very first Athlon CPU from AMD. Interesting enough this mode isn’t available on Core 2 Duo CPUs manufactured under 65-nm process –
i.e., model numbers starting with "4" or "6" –, but these CPUs implement other "extended" states (C1E and C2E) mentioned before. Core 2 Duo manufactured under 45-nm process – i.e., model numbers starting with "7" or "8" – do have this mode back again.

As we explained, when the CPU is in the Halt (C1) or in the Stop Grant (C2) states the CPU internal clock is cut from almost all units inside the CPU, making them to stop and thus consume less power. On these states, however, two internal CPU units are kept running: the bus interface unit and the APIC, Advanced Programmable Interface Controller. These units are kept running so the CPU can deal with important requests coming from the CPU external bus and can handle interruptions.

The next state, Sleep (C3), cuts all internal clock signals from the CPU, including the clocks from the bus interface unit and from the APIC. This means that when the CPU is in the Sleep mode it can't answer to important requests coming from the CPU external bus nor interruptions.

Intel CPUs and Turion 64 from AMD allow a C3 sub-mode called Deep Sleep, where the CPU external clock is also stopped, thus saving more power.

The way the CPU enters C3 state depends on the manufacturer. Intel CPUs add an extra pin, called SLP (or DPSLP, depending on the CPU model), which must be activated when the CPU is in C2 state in order to switch the CPU into C3 state. So first STPCLK pin must be activated and then one should activate the SLP pin. Entering the Deep Sleep state is achieved by simply cutting the external clock signal.

On AMD CPUs the C3 state is entered by simply reading a register from the ACPI (Advanced Control Power Interface), circuit that is physically located on the chipset. If the program, reads the PLVL_2 register, the chipset will activate the STPCLK pin putting the CPU into Stop Grant (C2) mode while if the program reads the PLVL_3 register the chipset will activate the STPCLK pin putting the CPU into Sleep (C3) mode.

AMD mobile CPUs (Turion 64) support a sub-mode called AltVID that allows the reduction on the CPU voltage while they are in the C3 mode.

Also don't forget that Turion 64, 65-nm Athlon X2 and Phenom CPUs also have a mode called C1E that isn't related to Intel's C1E that puts the CPU in a mode identical to C3. The difference between AMD's C1E and C3 states is basically how the CPU enters the Sleep state: while on the traditional C3 state the CPU must be put in that state usually by a command issued by the operating system, on C1E the CPU enters the Sleep state automatically when all cores are at Halt (C1) state.

C4 State

Modes C1, C2 and C3 deals basically with the clock signal. Since on C3 mode all clock signals inside the CPU can be stopped, there is no other way to save power by playing with the CPU clock signals. The next step on reducing the CPU idle power is to reduce the CPU voltage. Since power is directly proportional to voltage (P = V x I) if we reduce the CPU voltage we also reduce the amount of power being wasted.

The first mode to implement voltage reduction is called C4 or Deeper Sleep State and was first implemented on the Pentium M processor (i.e., Centrino platform), which was a CPU targeted to the mobile market, where power saving is extremely important to extend battery life. This mode is also available on Core Solo, Core Duo (the dual-core version of Pentium M), on all mobile versions of Core 2 Duo and desktop Core 2 Duo models with model numbers starting with "7" or "8" (i.e., 45-nm CPUs). This mode isn't available on 65 nm desktop Core 2 Duo CPUs (models starting with "4" or "6"). This mode is also available on AMD's Turion 64 processor.

Deeper Sleep State is achieved from Deep Sleep state, i.e., the CPU must first enter Deep Sleep State (C3) and then, from there, it can reduce its internal voltage. On Core Duo CPUs this must be done by activating a pin on the CPU called DPRSTP.

Just for you to have some real examples of how C4 state can save energy, let's consider mobile Core 2 Extreme X9100. In normal (C0) mode working at its full clock this CPU has a maximum current consumption of 59 A, which drops to 12.2 A when the CPU is in C4 state, a 79.32% reduction in consumption. On a mobile Core 2 Duo T9400 or T9600, which have a maximum current consumption of 47 A, maximum current consumption drops to 11.7 A when the CPU is under C4 mode, a 75.11% decrease in consumption.

Core Solo, Core Duo (the dual-core version of the Pentium M targeted to the mobile market and codenamed...
Yonah) and the 45-nm version of the mobile Core 2 Duo (i.e., models with numbering starting with 8 or 9 and the 7350 model) have another C4 mode, called Enhanced Deeper Sleep or simply C4E, which allows the CPU voltage to be reduced even more after the L2 memory cache has been disabled. This mode isn’t available on other CPUs. This mode is also called C5 by some people, even though this isn’t the real name of this mode.

Let’s give some examples of power savings brought by C4E state. First let’s consider mobile Core 2 Extreme X9100. In normal (C0) mode working at its full clock this CPU has a maximum current consumption of 59 A, which drops to 11.7 A when the CPU is in C4E state, an 80.17% reduction in consumption. On a mobile Core 2 Duo T9400 or T9600, which have a maximum current consumption of 47 A, maximum current consumption drops to 10.5 A when the CPU is under C4E mode, a 77.66% decrease in consumption.

C6 State

This is the latest addition on power saving, introduced with the 45-nm version of the mobile Core 2 Duo – i.e., models with numbering starting with 8 or 9 and the 7350 model. It is important to note that the desktop version of the 45 nm version of the desktop Core 2 Duo does not bring this functionality, which is also known as Deep Power Down.

When the CPU enters this state it saves its entire architectural state inside a special static RAM, which is fed from an independent power source. This allows the CPU internal voltage to be lowered to any value, including 0 V, which would completely turn off the CPU when it is idle. Then when the CPU is waked up it loads the previous state of all internal units from its special static RAM. Of course waking up the CPU from this state takes a lot longer than the previous states we discussed, but it is faster than turning off the computer and then turning it back on and loading the operating system, etc.

Notice that there is only one voltage line for the entire CPU (the only component with a different voltage source is the abovementioned special memory) and lowering or turning off the CPU voltage is an all-or-nothing kind of deal: if you turn off the CPU, you have to turn off it entirely when it goes into C6 mode.

The forthcoming Core i7 CPU (codename Nehalem) will have an embedded power control unit that allows the voltage for individual parts of the CPU to be reduced or turned off. For example, if only one processing core of the CPU is idle, it will be able to turn off just one of the cores, putting it on C6 mode. On current 45-nm mobile Core 2 Duo CPUs you can’t do that.

In order to enter C6 state the CPU must enter first into C4 state and from there switch to C6 state.

Let’s give some examples of power savings brought by C6 state. First let’s consider mobile Core 2 Extreme X9100. In normal (C0) mode working at its full clock this CPU has a maximum current consumption of 59 A, which drops to 11 A when the CPU is in C6 state, an 81.35% reduction in consumption. On a mobile Core 2 Duo T9400 or T9600, which have a maximum current consumption of 47 A, maximum current consumption drops to 5.7 A when the CPU is under C6 mode, an impressive 87.87% decrease in consumption.