CSE 520

Directory based cache coherence protocol

- Total memory = N x S
- Size
- Global mapping on physical processors
- Maintains the caching status of each location (blocks) mapped to P_i

<table>
<thead>
<tr>
<th>Status Shown</th>
<th>Data Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>D</td>
</tr>
<tr>
<td>W</td>
<td>U</td>
</tr>
<tr>
<td>S</td>
<td>I</td>
</tr>
</tbody>
</table>

Local cache status:
- Modified (exclusive): DM
- Valid: DU, DS
- Invalid: DI

Update cache status:
- Data value reply
- Update memory
- Directory state

Request to Uncached block on D2
- P_i has the block
- Excluse State
- P_i has the block in shared state
- Data with back
FSM for Simple Directory Protocol (Pg 234)
directory controller (Page 240)

Cache controller (Pg 211)

**State Diagram:**
- I: Initial state
- S: State after read
- M: State after write
- N: State after fetch
- U: State after invalidate

**Transitions:**
- CPU read hit -> S
- CPU read miss -> I
- CPU write hit -> M
- CPU write miss -> N
- Send rd miss msg -> I
- Send wr miss msg -> N
- Data write back -> S
- Data write back -> M
- CPU read miss -> U
- CPU write miss -> U
- Fetch -> I
- Invalidate -> I
- Write miss (from P) -> M
- Write miss (from N) -> U
- Read miss -> S
- Read miss -> U
- Data value reply -> S
- Data value reply -> U
- Share = {P} -> S
- Share = {Q} -> U

**Events:**
- Fetch/invalidate
- Data value reply
- Share = {P}
- Share = {Q}