Adaptive Mechanisms for Managing Cache Hierarchies in Chip Multiprocessors

CSE 520 Project Presentation
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Current trend of CMP Cache

• Massive multicore chips in future (32 cores)
• Private L1 and L2 caches for each core, forming a tile
• Many memory references have the potential to be resolved on-chip
• Adding cache hierarchy reduces AMAT
CMP cache solutions proposed

This paper proposes following solutions

- Use of L3 cache as victim cache for evicted lines from L2
- Use peer caching at L2
- Maintain reuse history for replaced lines for selective snarfing
- No writeback if clean line has multiple copies in L2 or in L3
Results so far . . .

- Test Input1 with Baseline
- Test Input1 with new protocol
- Test Input2 with Baseline
- Test Input2 with new protocol

Bar chart showing:
- Read Miss
- Write Miss
- On Chip Reads

Categories:
- Test Input1 with Baseline
- Test Input1 with new protocol
- Test Input2 with Baseline
- Test Input2 with new protocol
What remains . . .

- Use L3 as victim cache, this will further reduce AMAT
- Implement history table for L2 snarfing
- Run analysis on more memory access traces if possible
- Analyse the results and quantify reduction in memory access times using the access times numbers from the paper which the project is based on