This paper proposes a technique for reducing leakage power in caches by putting the cold cache lines into a state preserving low-power drowsy mode. The paper then investigates policies and circuit techniques for implementing the proposed idea with minimum performance loss and maximum savings in leakage power.

Strengths of the Paper:

1) The authors have compared two other techniques (gated VDD and ABB-MTCMOS) and have proposed a technique that uses the advantages of both the techniques and attains a reasonable compromise between the two.

2) According to the authors, the technique is much simpler and less complicated to implement than the other two techniques available.

Weaknesses of the Paper:

1) The authors have run a separate HSPICE simulation to study the effects of varying the power supply voltage, on leakage power, but the authors have not explained how they have setup the simplescalar simulator to simulate the proposed drowsy cache technique.

2) There is no clear explanation on how the results were obtained from the benchmarks. The authors have provided an equation to calculate the worst case execution time, but they have not clearly stated if they are using this equation to derive the results from the benchmarks. Also, there is no clear rationale on how the authors have arrived at the given equation.

3) This technique is very susceptible to Single Event Upsets (SEU) from alpha particles, as in the drowsy state; the voltage supply is very low.

4) Also, the power supply is dependent on process variations. Fixing this problem could be a topic for future research.