Critique by – Pravin Dalale (1200551200) Presented by – James Coleman
Title of Paper - Facilitating Efficient Synchronization of Asymmetric Threads on Hyper-threaded Processors

Paper is about –
In this paper the authors propose a way to utilize the MONITOR/MWAIT instructions introduced by Intel to accomplish thread synchronization. The work focuses on the asymmetric workloads and hyper threaded processor. Initially the authors quantify the performance of the MONITOR/MWAIT primitives by setting metrics such as source consumption and responsiveness. The results are then compared with existing schemes. The n they propose a frame-work through which one can use these privileged instructions to build condition-wait and notification primitives, with the least possible kernel involvement. Finally, they claim to have achieved a performance 12% better than that of the pthreads and 26% better as compared to the spin-loops-based implementation.

Strengths of the paper-
1. In case we consider the throughput as the performance metric the scheme proposed by the authors has shown on an average 20% improvement (fig.4) as compared to pthreads as well as the spin-loops. This is considerable improvement as there are very few papers in the contemporary architecture which claim this great an improvement, especially over pthreads.
2. This paper suggests mainly utilization of existing primitives to build new barriers and notification primitives using existing MONITOR/MWAIT instructions. This is considerable achievement as there are no hardware modifications associated with this scheme. As far as the deployment of this scheme or framework is concerned it is very cost effective.
3. The concept introduced in the paper can be easily extended to the multiprocessor systems.
4. The scheme proposed by the authors is very easily deployable in the MPI like framework.

Weaknesses of the paper-
1. The scheme introduced in the paper is limited only for workloads which are asymmetric in nature.
2. The scheme in the paper is limited only for the hyper threaded processors.
3. In case there are different primitives other than the MWAIT/MONITOR then it involves greater understanding of the the nature and functioning of those primitives to come up with a framework to extract same performance improvements.
4. The results show that the miss coverage of the pthreads is better than the scheme proposed by the authors.
5. The cycle breakdown results show that pthreads are as good as the scheme proposed by the authors. Hence if the nature of workload is a mixture of symmetric and asymmetric then the overall speedup of pthreads is bound to be better than the proposed scheme.