Finite State M/c Specification of MSI Bnooping Cache Coherence Protocol

Cache State transitions based on request from CPU.

Invalid

CPU read

Place read miss on bus

CPU write

Place write miss on bus

Modified Exclusion (read/write)

CPU read hit

Shared (read only)

CPU read miss, with block

Place read miss on bus

CPU write miss

Place write miss on bus

CPU write miss

Write back cache block

Place write miss on bus

Cache State transitions based on requests from the bus

Invalid

Write miss for this block

Invalidated for this block

Shared

Read miss for this block

Exclusive

Write back block

Fig 4.6. (Computer Arch. O.A.) p 214