Computer Architecture I (CSE 420/CSE 598) (Fall 2008)
Quiz 3 (Memory Hierarchy – Single and Multiprocessor) Points (20 points)

NAME: ID:

1. [5] If the virtual address space is 4GBytes, each page size is 4KBytes, and physical memory size is 2MBytes, what is the size (in terms of bits – not number of entries as in Q2) of first level and second level page table in a two-level page table scheme with the second level page table with 1M entries? Assume each second level page entry stores a valid bit, two bits for access permission, and the physical page address.

2. [3] Assume cache miss penalty is 200 clock cycles and all instructions normally take 1.0 clock cycle (ignoring memory stalls). Assume the average miss rate is 2% and there is an average of 1.5 memory references per instruction. For a given program:
   a. Calculate the CPU time without cache
   \[
   \text{CPU time} = \frac{1C}{(CPI + MR \times Mem. Rate \times MP) \times CC} \\
   IC(1 + 1.5 \times 200) \times CC = 701 + IC \times CC
   \]
   b. Calculate the CPU time with cache
   \[
   IC(1 + 0.02 \times 1.5 \times 200) \times CC = 7IC \times CC
   \]
   c. Calculate the CPU time with perfect cache (100% hits)
   \[
   IC \times CC
   \]

3. [3] Remember that AMAT = Hit time + Miss rate * Miss Penalty. What is the effect (positive, negative or neutral) of multilevel caches on each of the three terms in the expression of AMAT? Explain your answer.

Hit time - neutral - only depend on cache organization of 1st level cache - which I is not changed
Miss Rate - neutral - S size - which is not changed
Miss Penalty - positive - it reduces access time of intermediate key level is substantially less than MP.

What if 2nd level page table size is 1K entries?

- 105 bits
- 12 bits
- Second level page table
- 2nd level size = 2^10 x 12 bits
- 1st level = 2^10 x 32
4. [4] Suppose you want to add "owned" (O) state to the simple directory protocol discussed in the class. Show the state transition between the M and O state for
   a. cache controller
   ![Diagram](image)
   b. directory controller
   ![Diagram](image)

5. [3] In AMD Opteron microprocessor, the first level cache is 64Kbytes with 64 byte blocks and 2-way set associative placement. Further, the physical address size is 40 bits.
   a. Give the index size for this scheme
   \[ \text{# of sets} = \frac{\text{# of blocks in cache}}{\text{associativity}} - 9 \text{ bits} \]
   ![Diagram](image)
   b. Give the tag size for this scheme
   \[ \text{tag size} = 40 - 11 = 25 \text{ bits} \]
   ![Diagram](image)
   c. What will be the index size and the tag size if the scheme is changed to 4-way set associative?
   - Index: 8 bits
   - Tag: 26 bits
   - 24 bits
   ![Diagram](image)

6. [2] Given the data below, what is the impact of second-level cache associativity on its miss penalty?
   Hit time L2 for direct mapped = 10 clock cycles
   2-way set associativity increases hit time to 10.1 clock cycles
   Local miss rate for L2, direct mapped = 25%
   Local miss rate L2 for 2-way set associative = 20%
   Miss penalty L2 is 200 clock cycles

   \[ MP_{L2} = HT_{L2} + MR_{L2} \times MP_{L2} \]
   \[ MP_{L2, \text{direct}} = 10 + 25\% \times 200 = 60 \text{ cc} \]
   \[ MP_{L2, \text{2way}} = 10.1 + 20\% \times 200 = 50.1 \text{ cc} \]