Quiz on Monday! on Caching

Midterm Oct 15th
- Closed Book
- Closed Notes
- Closed Neighbor
- Closed Phone (No texting)

1. Understand the concept
   - there will be some short answer questions testing
   - the concepts

2. Some numerical problems
   - bring your calc.
   - show all your work
   - to get partial credit

Study the notes - sections of book & the slides.
D₁, ..., Dₙ are the subdirectories.

Address Space

for each block in P₁’s memory
maintain its
state information

may be cached in
say P₃ & P₄

→ Shared

→ 1 bit map

→ Set of processors which have cached copies

→ Which directory

See 4.4
Local node wants a block from P1's memory.

Node generating the address (say A) to node having information of A.

Remote node having latest copy of A.

Data.
Fetch invalid
Data write back

Invalid
CPU rd. (A)
Send rd. miss
to home dir. of A
CPU wr.
Send wr. miss
to home dir. of A
CPU wr. hit
Send wr. miss
CPU wr. miss
Send wr. miss

Shared
CPU rd. hit
Send Rd. miss
msg. to dir. of A
CPU rd. miss
Send rd. miss
msg. to dir. of A

Exclusive
CPU wr. hit
Send wr. miss
Data write back
Write miss \(\rightarrow\) home dir. of addr.
being accessed.

Frame
Block
Exc.

CPU wr. hit
Send wr. miss
Uncoheld

Data value reply

Read miss
(from proc. P)

Exclusive

Data value reply

Write miss from Q

Fetch/Inv to P;
Data reply to Q

Assuming
Share = \{P\}

Shared

Data value reply

Read miss

Share = Share \cup \{P\}

Share = \{Q\}

Assuming
Share = \{P\}

Before write miss.