Instruction-Level Parallelism (ILP)
Task-level Parallelism
Data-level Parallelism

fully parallel code
Add A, B, C
Add D, E, F

Flynn's Classification
SIN (Single Instruction, Multiple Data)
MIMD: seq. computer
SIMD: parallel processor
hyperscalar

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Advantage of Pipelining:

\[ \text{Speedup} = \frac{T_{np} + T_p}{T_{np}} \]

\[ T_{np} \]

\[ T_p \]

Speedup is \# the optimized program.

Speedup is the improvement factor of an optimized (pipelined) program w.r.t. the non-optimized (non-pipelined) program.

\[ \text{Speedup} = \frac{T_{np}}{T_p} \]

(e.g., \( \frac{20s}{5s} = 4 \))

Suppose you have an n-stage pipelined processor. What is the maximum speedup that can be achieved?
What will be time required to complete m instr.

What we have taken

but in reality nats > t

= m * t

Speedup: \[
\frac{\text{nats}}{\text{nats} + (m-1)t_s}
\]

\[
\approx \frac{n}{t}
\]

In each instr will take = nats

1st instruction will get completed at nats
each subsequent instr finishes in subsequent cycles.

Time to complete m instr = nats + (m-1)t_s